WS 2021/2022 14.12.2021

Exercises to the lecture
Complexity Theory
Sheet 4

Prof. Dr. Roland Meyer
Thomas Haas

Delivery until 10.01.2022 at 12:00

Exercise 4.1 (Collapse of the Polynomial Hierarchy)

In this exercise, we prove what is sufficient for a collapse of the polynomial hierarchy.

a) Assume we have an $i \in \mathbb{N}$ so that $\Sigma_i^{\mathsf{P}} = \Sigma_{i+1}^{\mathsf{P}}$. Show that $\Pi_i^{\mathsf{P}} = \Pi_{i+1}^{\mathsf{P}}$.

b) Prove the following: If we have an $i \in \mathbb{N}$ with $\Sigma_i^{\mathsf{P}} = \Pi_i^{\mathsf{P}}$, then for any $i' \geq i$ we have that $\Sigma_{i'}^{\mathsf{P}} = \Pi_{i'}^{\mathsf{P}} = \Sigma_i^{\mathsf{P}}$. Hence, the polynomial hierarchy collapses to the i-th level.
Hint: Prove the statement by an induction on i'. For the induction step, make use of the fact that $\Sigma_{i'+1}\mathsf{QBF}$ is $\Sigma_{i'+1}^{\mathsf{P}}$-hard.

c) Show that the existence of an $i \in \mathbb{N}$ with $\Sigma_i^{\mathsf{P}} = \Sigma_{i+1}^{\mathsf{P}}$ is already sufficient to cause a collapse of the polynomial hierarchy to the i-th level.

Exercise 4.2 (Unbounded Fan-In)

Let g be a gate in a circuit. The *Fan-In* of g is the indegree of g, the number of incoming edges. A circuit has Fan-In *bounded by* $k \in \mathbb{N}$ if for any gate, the Fan-In is bounded by k. In the definition of NC, we restricted to circuits of Fan-In bounded by 2. In this exercise, we show that the restriction is reasonable.

Let C be a circuit of unbounded Fan-In with n input variables. Let $\text{size}(C) = s(n)$ and $\text{depth}(C) = d(n)$. Show that there is a circuit C' that has Fan-In bounded by 2 and

- $C'(x) = C(x)$ for all inputs x,
- $\text{size}(C') \in \mathcal{O}(s(n)^2)$, and
- $\mathit{depth}(C') \in \mathcal{O}(d(n) \cdot \log s(n))$.

Deduce that $\mathsf{AC}^i \subseteq \mathsf{NC}^{i+1}$.

Exercise 4.3 (Addition with parallel carry computation)

In this exercise we want to solve the *addition problem* using circuits:

Addition (ADD)	
Input:	$2n$ variables $a_1, \dots, a_n$ and $b_1, \dots, b_n$, the binary representation of the two natural numbers a and b.
Question:	Output the $n+1$ variables $s_1, \dots, s_{n+1}$ that represent $s = a + b$.

A first approach to this problem would use *full adders*. A full adder for the i-th bits would compute $a_i + b_i + c_i$, where c_i is the carry. The adder would output the sum bit and a new carry bit. This new carry bit could then be used as input for the full adder for the $(i+1)$-st bits. Seen as a circuit, this would have depth $\mathcal{O}(n)$. We want to do better:

a) Construct a circuit C_i of unbounded Fan-In that computes the i-th carry bit c_i, has size $\mathcal{O}(i)$, and constant depth.
Hint: In contrast to the circuit described above, the computation of c_i should not depend on c_{i-1}. Note that c_i is 1 if and only if there is a position $j < i$, where the carry is generated and propagated to position i. Construct a Boolean formula for this condition - this may also depend on $a_1, \dots, a_{i-1}$ and $b_1, \dots, b_{i-1}$. Then transform the formula into a circuit.

b) Use Part a) to construct a circuit for ADD that has size $\mathcal{O}(n^2)$ and constant depth.

c) Conclude that there is a circuit of Fan-In bounded by 2 that decides ADD, has polynomial size, and logarithmic depth.

Exercise 4.4 (Logspace reductions and the class NC)

Let A, B be two languages so that $A \leq_m^{log} B$ and $B \in \mathsf{NC}$. Show that A is in NC.

Delivery until 10.01.2022 at 12:00 to `https://cloudstorage.tu-braunschweig.de/preparefilelink?folderID=2UBADHPF6dDgmphBeAHkK`.