

Intuition to the construction from last time:

The construction makes heavy use of the following trick in automata theory:

to shuffle two languages $L(M_1)$ and $L(M_2)$ over disjoint alphabets $\Sigma_1 \cap \Sigma_2 = \emptyset$,

extend M_1 by loops Σ_2 on each state,

and M_2 by loops Σ_1 .

The resulting automata M_1' and M_2' satisfy

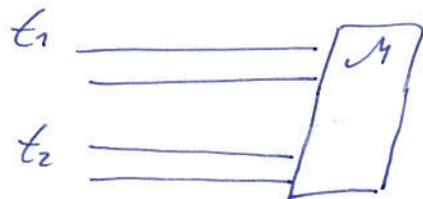
$$L(M_1') \cap L(M_2') = L(M_1) \cup L(M_2).$$

Example:

$\{abc\} \cup \{xyz\}$

$$= L\left(\begin{array}{c} x,y,z \\ \text{---} \end{array} \begin{array}{c} a \\ \text{---} \end{array} \begin{array}{c} b \\ \text{---} \end{array} \begin{array}{c} x,y,z \\ \text{---} \end{array} \right) \cap L\left(\begin{array}{c} a,b \\ \text{---} \end{array} \begin{array}{c} x \\ \text{---} \end{array} \begin{array}{c} y \\ \text{---} \end{array} \begin{array}{c} z \\ \text{---} \end{array} \begin{array}{c} a,b \\ \text{---} \end{array} \right).$$

- 1.) The memory sees a shuffle of the stores from both threads:



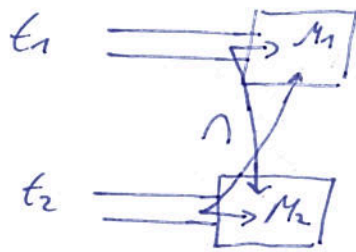
For example, the memory may see

$$S = s(a, 1, t_1). s(b, 2, t_2). s(a, 2, t_1).$$

- 2.) Using the above idea,

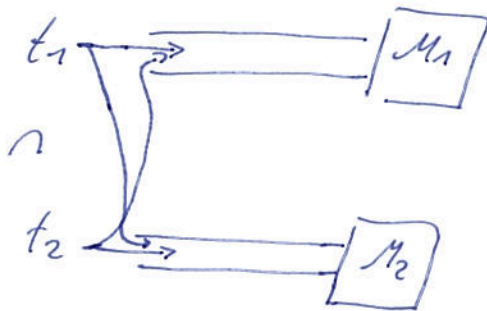
the shuffle can be obtained

by synchronizing (intersection) the two automata $t_1 \equiv \boxed{M_1}$ and $t_2 \equiv \boxed{M_2}$ on the memory updates:

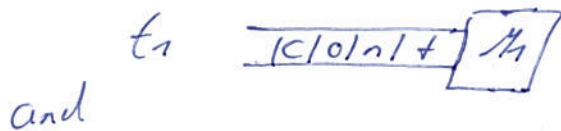


Here, one really defines alphabets (Σ_i consists of stores $s(t_i, v_i)$, $i=1,2$) and applies the loop trick.

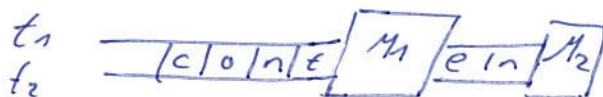
- 3.) Since the channels are FIFO, the stores leave the buffer in the order in which they were put into the buffer. So instead of guessing the buffered stores of t_2 at the memory, thread t_1 guesses the stores of t_2 already when inserting commands into the buffer:



- 4.) Now the content of both buffers is identical, up to the fact that M_1 and M_2 process the buffer at different speed:



can be understood as one buffer with two pointers:

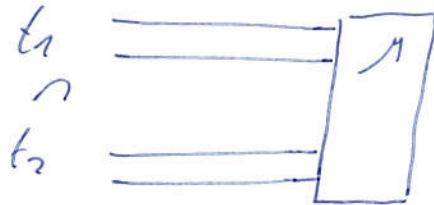


Remark:

One may think that it should be sufficient to guess the sequence of memory updates

$$S = st(a, 1, t_1). st(b, 2, t_2). st(a, 2, t_1)$$

and write this shared sequence into both buffers:



This, however, yields a strict under-approximation of TSO.

TSO requires that sequence S results from store actions leaving the buffer.

The above model additionally enforces this order when the stores are sent to the buffer.

↳ This is more than TSO asks for.

↳ That the two memories can process the shared buffer at different speed fixes the problem.